

Design and Assessment of Type-II PLL implementing Various CMOS PFDs

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Abstract

This paper reflects the design and comparison of different Phase Frequency Detectors (PFD) used in Phase Locked Loop (PLL) using different logic gates. A PFD plays a major role in PLL, it detects both phase and frequency of a signal. In this paper a PFD is implemented using three different gates like AND, NOR and NAND gates. An AND based PFD produces accurate results and eliminates the missing edge and phase ambiguity problems, where NAND based PFD generates moderate output and it can be implemented using less number of transistors so the power dissipation will be less when compared with the AND based PFD but the RMS noise is high. Finally by using the NOR based PFD generates accurate results with less power dissipation and reduced RMS noise and it eliminates the missing edge and phase ambiguity problems. In this paper three PFDs are compared in terms of quality of the output, power dissipation and the RMS noise. These PFDs are implemented in Type-II PLL with design of charge pump, low pass filter and voltage controlled oscillator. The parameters calculations and the observation of waveforms are done using the Mentor Graphics Tool.

Keywords: Phase Frequency Detector; Phase Locked Loop (PLL); Root Mean Square Noise (RMS Noise)

Introduction

A phase-locked loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. It consists of a phase detector, low pass filter and a VCO as shown in figure 1[14]. It selects the intended channel with minimum distortion. The phase detector is a circuit that normally has an output voltage with an average value proportional to the phase difference between the input signal and the output of the

VCO. It is used as an “error amplifier” in the feedback loop thereby minimizing the phase difference. An Exclusive-OR (XOR) logic gate can be used as a phase detector. The low-pass filter is used to extract the average value from the output of the phase detector [1] [2]. This average value is then amplified and used to drive the VCO. The negative feedback of the loop results in the output of the VCO being synchronized with the input signal. Depending on the type of the phase-locked loop, the output of the oscillator may or may not have a phase difference compared with the phase of the input signal. It is used in CMOS transceivers for tuning of signals [3][4]. The figure 1 represents the phase detector which generates pulses at regular intervals of time due to which a finite phase error exists. To nullify this error, we must change the frequency of the VCO or allow the VCO to accumulate phase faster (or more slowly) than the reference so that the phase error vanishes or change the frequency back to its initial value. Basically for practical circuits, negative feedback loop is used. The PD produces repetitive pulses at its output, modulating the VCO frequency and generating large sidebands, so we interpose a Low Pass Filter in between phase detector and voltage controlled oscillator to suppress these pulses. The combination of phase detector and low pass filter is replaced by a frequency detector that generates a dc value in proportion to the input frequency difference. The PLL may also suffer from a finite error if its loop gain is finite or if the frequency detector exhibits offsets. Hence type-I PLL suffers drawbacks like less stable loop, limited acquisition range and finite static phase error and its variation with input frequency. As an alternative, we use type-II PLL practically which is shown in figure 2. It consists of a PFD, Charge pump, Low Pass Filter and Voltage Controlled Oscillator.

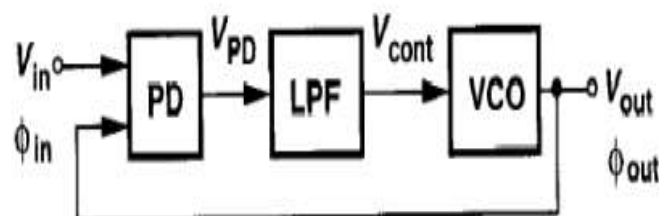


Figure 1. Basic Architecture of PLL

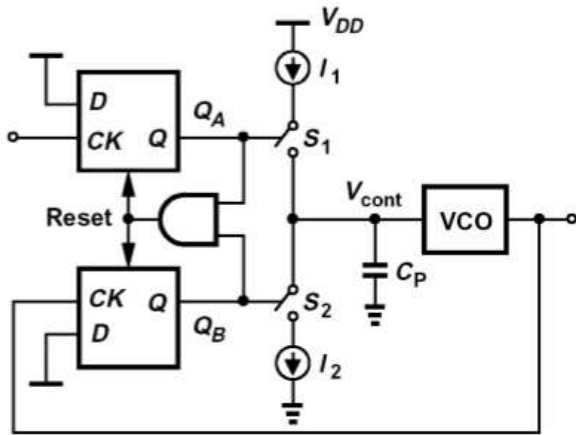


Figure 2. Type-II PLL Implementation

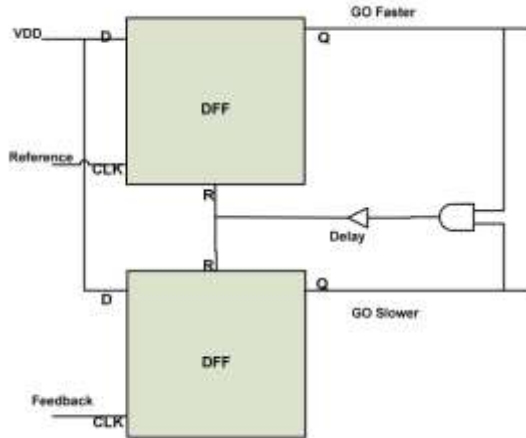


Figure 3. Block diagram of a PFD

A Phase Frequency Detector [6][12][13][14] (PFD) is typically an error amplifier. It compares the phases of the input and output signals and generates a corresponding error pulse. In the earlier design of the Phase Detector it can be thought of as an EX-OR gate which generates error signal or logic high if both the signals are at different level. This basic form of Phase Detector is not capable to detect large frequency differences, hence not used. Generally, the error pulse is named as UP and DOWN pulse for the purpose of simplicity[8][9]. If the phase difference between input and output is positive then the PFD generates an UP signal. More precisely if the reference signals phase (generally positive edge of clock/signal) leads the positive edge of the output signal then the PFD generates an error pulse proportional to the time delay between the two positive edges. Similarly if the feedback clocks/signal's positive edge is leading the reference clock's positive edge then the DOWN pulse is generated. The reader may wonder what effect has the UP and DOWN pulse on the loop dynamics and operation in general [6][7][11].

PLL Designs

The PLL designs are carried as discussed below. The charge pump is designed as shown in figure 4. It consists of two NMOS transistors that turn on when the QA and QB are active high. The active input for QA gives the output and the active input for QB gives the logic 0 as output constantly. The Low Pass Filter is designed as shown in figure 5. It consists of three PMOS and one NMOS transistors that work for LPF. The PMOS transistors act as a diode connected loads and the output is taken at drain of M3.

Assuming first for the sake of discussion that the Feedback clock runs at a high frequency than the reference, in order to match the “reference signals” frequency the Feedback clock must slow down, or the VCO must slow down as shown in figure 3. This can be made to happen if we can generate a driving voltage such that the VCO frequency scales down or slows down in order to match the reference. This difference in frequency or phase can be detected by only Phase Frequency Detector in the PLL system as only this block talks with both the signals. Therefore, this block should generate a signal to slow down the VCO frequency. The “DOWN” pulse is nothing but this signal which will order the VCO to step down its frequency or in other words to slow down. Similarly, an “UP” signal is generated to tell the VCO to catch with the reference in case its frequency has slowed down as compared to the reference clock. Having said so, we can now take a look at the general block diagram of the Phase Frequency Detector (PFD) [9][10][11] and then delve further deep to discuss the circuit diagram and to know how the previously explained statements are implemented.

The Voltage Controlled Oscillator is designed as shown in figure 6. It consists of five C²MOS inverters and one CMOS inverter forming a Ring Oscillator. The Phase of the inverters is such that fixed frequency oscillations are obtained.

The PFDs are designed using different logic gates i.e., by using AND gate, NAND gate and NOR Gate [5]. The internal structure is designed as cross coupled NOR Gates as shown in figure 7.

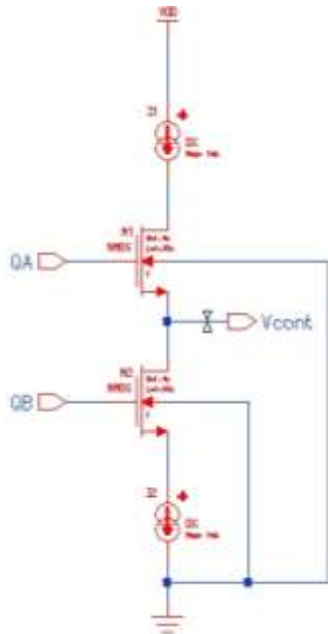


Figure 4. Charge Pump Design

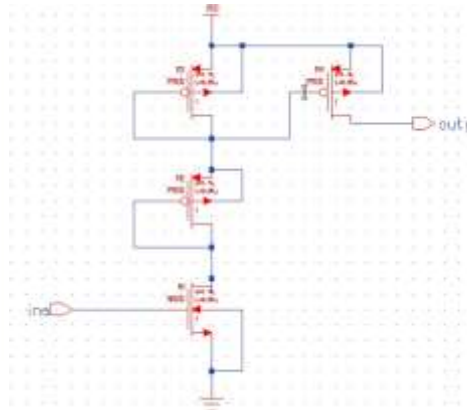


Figure 5. Low Pass Filter Design

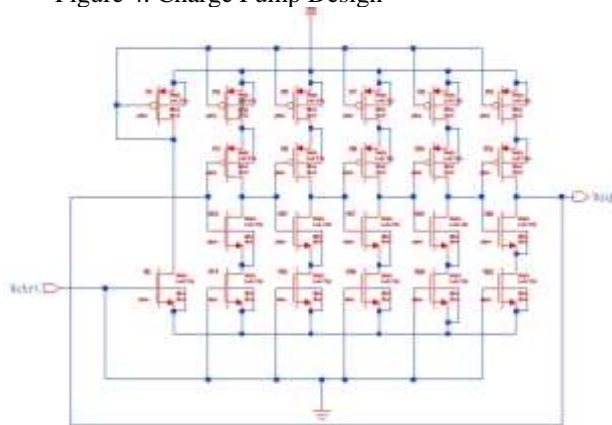


Figure 6. Voltage Controlled Oscillator

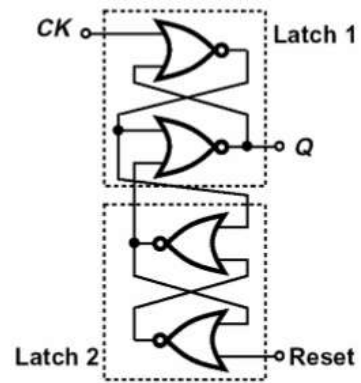


Figure 7. Internal Structure of D-Latch

Figure 8 shows the block diagram of the AND based Phase Frequency Detector where the PFD is implemented using AND gates and the transistor level diagram of AND based PFD is shown in figure 4 [6][7]. V_{ref} and V_{div} are the input signals. Here, V_{ref} is an input signal and the V_{div} is the signal coming from the VCO which is divided by the dividing block in the PLL so that small phases of the two signals can be compared to get accurate results.

To analyze the RMS noise the V_{div} is taken as a sine wave with 3.3V as amplitude with 150MHz frequency and the V_{ref} is nothing but a pulse signal with 3.3V amplitude and with a dc supply voltage of 3.3V. An AND based PFD [8] requires 22

transistors as shown in figure 9. Among the total number of transistors, 11 are PMOS transistors and 11 are NMOS Transistors. The transistors width to length ratio is kept so as to satisfy the W/L ratio relation between PMOS and NMOS for symmetrical output signal swing.

The NAND PFD requires less number of transistors than the AND PFD so the power dissipation will be less than an AND PFD. The block diagram of an NAND PFD is shown in figure 10 and the number of transistors used by the NAND based PFD are 20 [6][9][10][15].

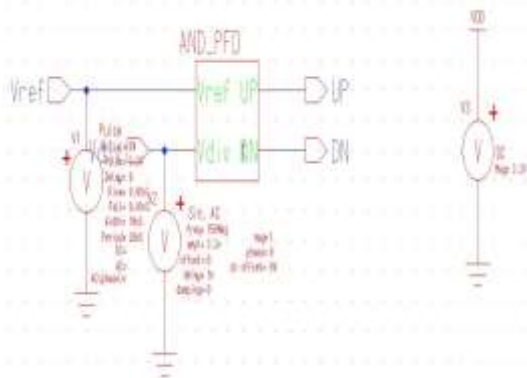


Figure 8. Block diagram of AND PFD

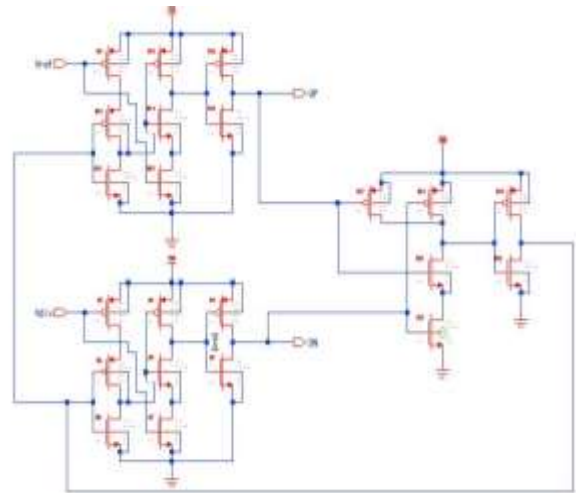


Figure 9. Transistor level diagram of AND PFD

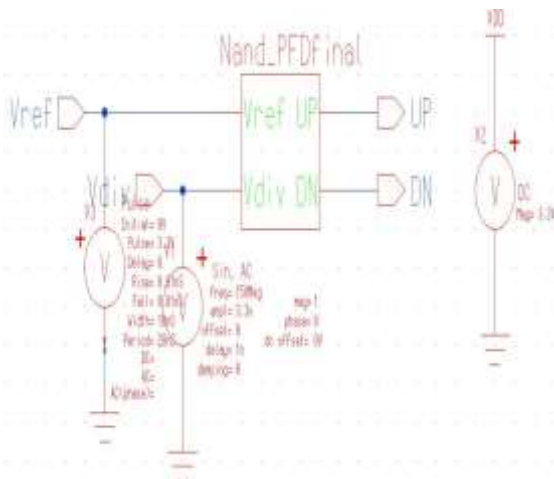


Figure 10. Block diagram of NAND PFD

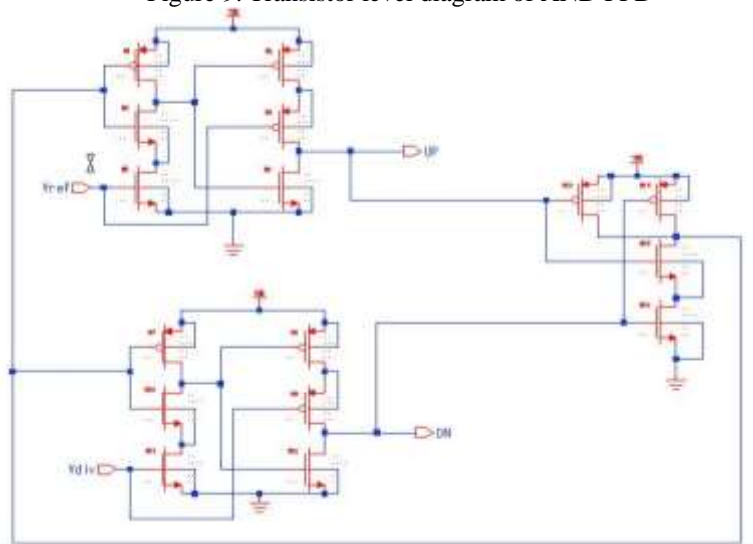


Figure 11. Transistor level diagram of NAND PFD

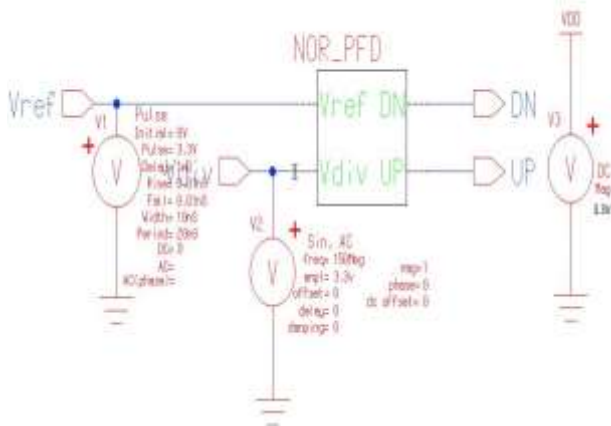


Figure 12. Block diagram of NOR PFD

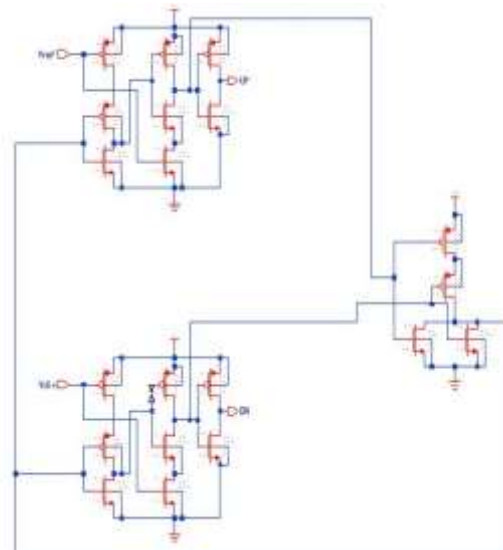


Figure 13. Transistor level diagram of NOR PFD

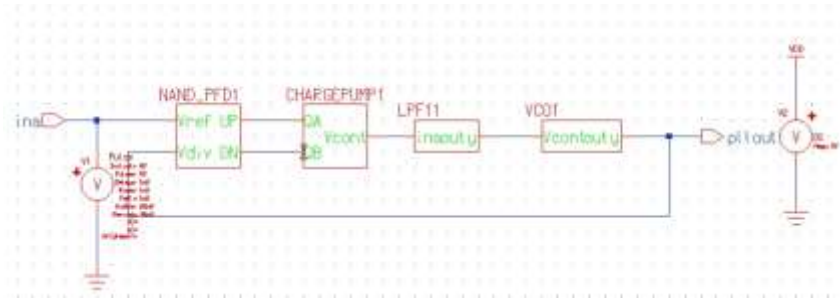


Figure 14. Type-II PLL with NAND PFD

The transistor level diagram of NAND PFD is shown in figure 11. For implementing this NAND based PFD, 16 Transistors are required. Among 16 transistors, 8 transistors are PMOS and the remaining 8 are NMOS transistors. The NOR PFD give better results in terms of power dissipation ,RMS noise and the output resultant waveforms when compared with the NAND and AND based PFDs. The block diagram of NOR based PFD is shown in figure 12. The transistor level diagram of NOR PFD is shown in figure 13. The optimized CMOS implementation of NOR PFD requires 20 MOSFETs among which 10 are PMOS and 10 are NMOS Transistors. The Type-II PLL is constructed using these circuits with various combinations of PFDs as shown in figure 14. In this design, the NAND PFD is replaced by AND PFD and NOR PFD.

RESULTS AND COMPARISON

The designs are simulated in Mentor Graphics Tools using 90nm CMOS Technology. The figures 15, 16 and 17 show the simulation results of the three PFD designs. The power

dissipation of AND PFD is $78.725\mu\text{W}$ and the RMS noises at V_{UP} and V_{DN} are 254.17 dB, 281.21 dB.

The simulation results of AND PFD are shown in figure 15 which shows accurate results when compared with the remaining two PFDs. The simulation results of NAND PFD are shown in figure 16. The NAND PFD dissipates the power of $76.165\mu\text{W}$ and the RMS noise of V_{UP} and V_{DN} are 324.67 dB, 318.37 dB. So, by using the NAND PFD the power dissipation will be reduced but the RMS noise will be more so the output wave will have the noise components.

The power dissipation of NOR based PFD is $73.725\mu\text{W}$ and the RMS noise of V_{UP} and V_{DN} are 177.04 dB and 161.78 dB. The NOR based PFD produces good results when compared with the NAND based PFD and very good improvement in terms of noise and power dissipation. The simulation results of the NOR PFD are shown in figure 17

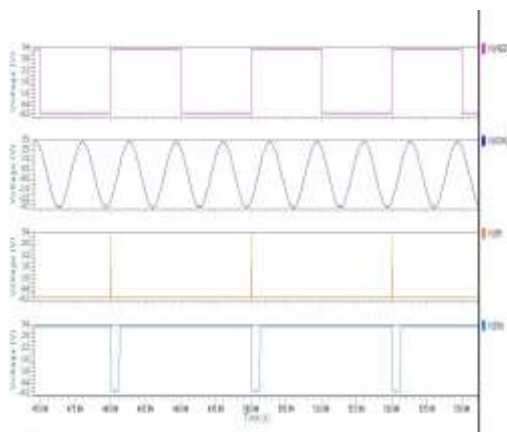


Figure 15. Simulation results for AND PFD

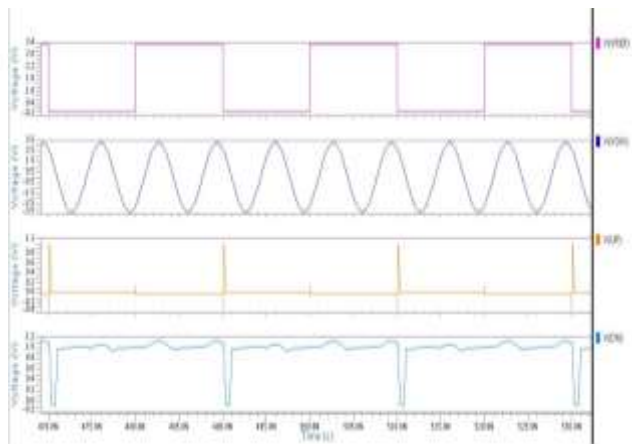


Figure 16. Simulation results for NAND PFD

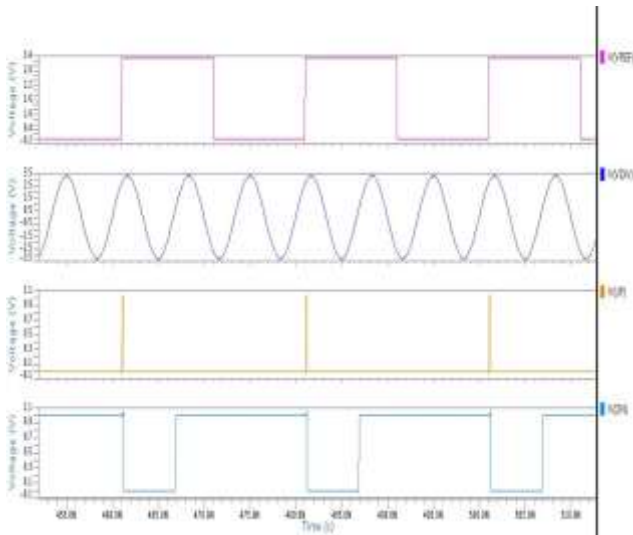


Figure 17. Simulation results for NOR PFD.

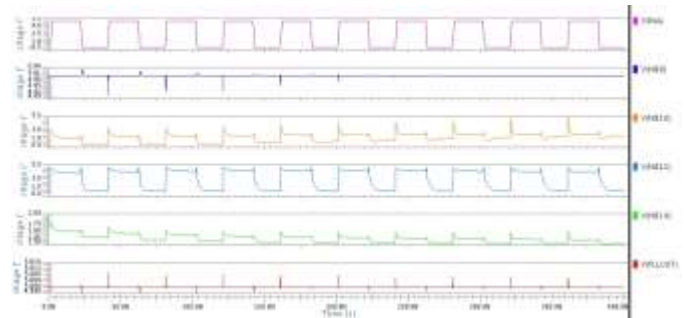


Figure 18. AND PFD Based PLL

TABLE I. COMPARISON OF THE DESIGNED PFDs

Type of PFD	Parameters			
	Output Quality	Power Dissipation (μW)	RMS Noise (dB)	
			V _{UP}	V _{DN}
AND PFD	Excellent	78.72	254.17	281.21
NAND PFD	Noisy	76.135	324.67	318.37
NOR PFD	Fair	73.725	177.04	161.78

Table 1 gives the comparison between three PFDs and their parameters like power dissipation, RMS noise, output results and the supply voltages. NOR PFD gives better results in terms of parameters, an AND PFD gives exact outputs and a NAND based PFD produces noisy results. So based on the type of application one can choose either AND PFD or NOR PFD. The NOR PFD offers less power dissipation of around

6% to that of AND PFD and 3% to that of NAND PFD. The RMS Noise was also reduced by 30% and 45% to that of AND PFD and NAND PFD respectively for V_{UP} and 42% and 49% to that of AND PFD and NAND PFD respectively for V_{DN}. Hence from table I, we conclude that among three PFDs the NOR PFD is better and if the exact results are needed then the priority will be given to And PFD.

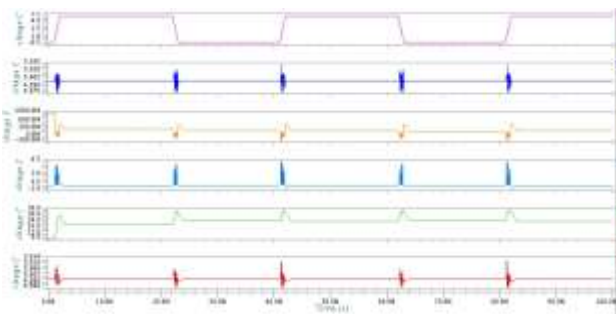


Figure 19. NOR PFD Based PLL

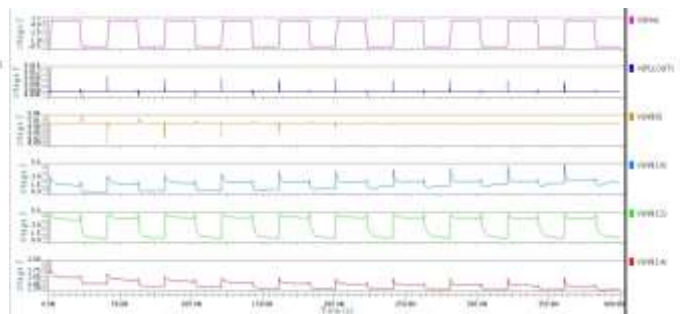


Figure 20. NAND PFD Based PLL

TABLE I. COMPARISON OF THE DESIGNED TYPE-II PLLS

Type of PLL	Parameters					
	Output Quality	Power Dissipation (mW)	Frequency (MHz)	Rise Time (pS)	Fall Time (pS)	Delay Time (pS)
AND PFD BASED PLL	Excellent	173.6067	24.993	66.848	20.036	353.2
NAND PFD BASED PLL	Good	64.5510	24.993	66.848	20.036	353.2
NOR PFD BASED PLL	Fair	129.6490	356.34	1010.8	1277.5	70.498

The PLLs are simulated for 90nm CMOS technology, the corresponding waveforms are shown in figures 18, 19 and 20. The NOR PFD based PLL simulation output is better in terms of amplitude but somewhat distorted. The output waveforms of NAND PFD based PLL are good in terms of output voltage and distortion. The output waveforms of AND PFD based PLL have better amplitude and less distortion. The NOR PFD

Conclusion

The PLL is the device used for tuning to the required frequency range of the receiver. It consists of three circuits, i.e., phase detector, low pass filter and a VCO. The Type-I PLL suffers from less stable loop, limited acquisition range and finite static phase error and its variation with input frequency. Hence Type-II PLL is considered for practical designs which has Phase Frequency detector, Charge Pump, Low Pass Filter and Voltage Controlled Oscillator. Among these PFD plays a important role, in extracting the phase of the receiving signal in line with the reference signal. A PFD is a circuit that senses two periodic inputs and produces an output whose average value is proportional to the difference between the phases of the inputs. Basically it is implemented by using XOR gate, but this gate consumes more area and power. This paper deals with design of PFD using three different logic gates like AND, NAND and NOR gates. The PFDs are operated at 150MHz frequency and with the supply voltage of 3.3V. To analyze the RMS noise the V_{div} is taken as a sine wave with 3.3V as amplitude with 150MHz frequency and the V_{ref} is nothing but a pulse signal with 3.3V amplitude

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based PLL has less delay than the other two designs. The corresponding rise and fall times are very large. But still the power dissipation is minimum in NAND PFD based PLL with 50.2% less than that of NOR PFD based PLL which is 25.3% less than that of AND PFD based PLL Hence depending upon the design, we choose the Type-II PLL.

and with a dc supply voltage of 3.3V. From results, it was observed that for accurate results, one can choose AND based PFD but it consumes more power. The NOR based PFD shows improved performance in terms of power dissipation and RMS noise. Even though the NOR PFD requires 22 transistors, it gives better in RMS noise suppression and reduction in power dissipation. The NOR based PFD also eliminates the missing edge and the phase ambiguity problems. The simulation results and the parameters are calculated using the Mentor Graphics tool at 90nm CMOS Technology. The NOR PFD offers less power dissipation of around 6% to that of AND PFD and 3% to that of NAND PFD. The RMS Noise was also reduced by 30% and 45% to that of AND PFD and NAND PFD respectively for V_{UP} and 42% and 49% to that of AND PFD and NAND PFD respectively for V_{DN} . If the accuracy and area occupied can be slightly ambiguous, then NOR PFD proves to be a best choice. The NAND PFD based PLL has optimum delay and less power dissipation i.e., 50.2% less than that of NOR PFD based PLL which is 25.3% less than that of AND PFD based PLL Hence for low power PLL designs, we choose the design of Type-II PLL

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